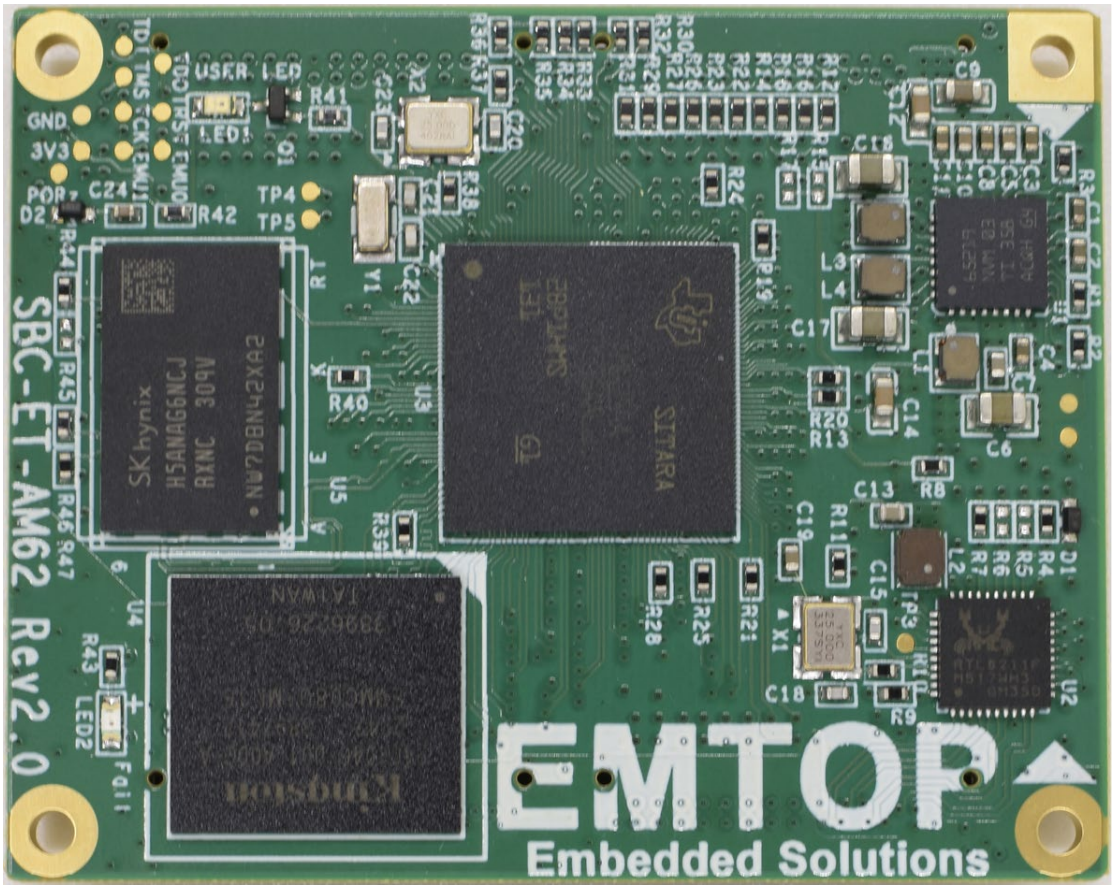
SOM-ET-AM62



Hardware User Manual

Version: 1.0

2024-09-19

Revision Record:

Version	Date	Description
1.0	2024-05-13	Trial Release

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1. Product Introduction

This section briefly describes the performance parameters and target application scenarios of the single-board computer SOM-ET-AM62 based on the TI AM623x/AM625x series CPU.

The SOM-ET-AM62 is a core board launched by Shenzhen EMTOP Technology Co., Ltd., based on the TI AM623x/AM625x series embedded CPU. It adopts a core board + baseboard design, with an ultra-small size of 50x40mm, complete interface design, and rich peripheral interfaces, facilitating users to directly integrate project development.

The TI AM623x/AM625x is a collection of high-performance, ultra-efficient processors, which is the latest high-performance, low-power processor collection launched by TI. It adopts up to 4x ARM Cortex-A 53 cores, with a maximum operating speed of 1.4G Hz, and integrates a Cortex M4F MCU with a frequency of up to 400MHz and an R5F real-time processing unit. The TI AM623x/ AM625x application processors include an integrated power management module, reducing the complexity of external power supplies and simplifying power-up sequencing, and a graphics processor (AM625x) compliant with OpenGL ES3.1 and Vulkan 1.2, along with a PRU subsystem. At the same time, the AM62XX integrates a rich set of peripheral resources, depending on the positioning of the CPU sub-model, with up to 1 *LCD controller, 1* LVDS, 2 *RGMII, 2*OTG interfaces, 3* CAN -FD, 1 *CS interface, 3*SPI, 3*SDIO, 9*UART, 6*I2C, 5*SPI, 3*MCASP, 3*PWM, and 2x PRU subsystems.

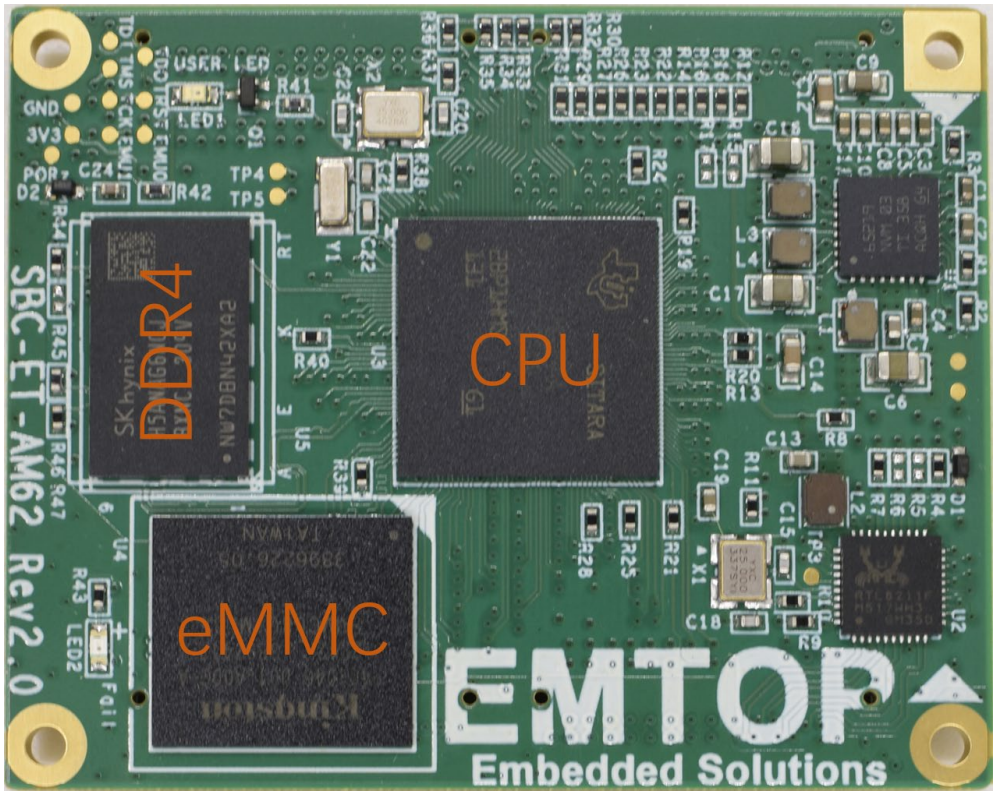
The EVK -ET-AM62 is a high-cost performance, easy-to-use, and stable development kit designed by Shenzhen EMTOP Technology Co., Ltd. based on the interface characteristics and function definitions of the TI AM625x and AM623x series CPUs. The target application scenarios are as follows:

- IoT Gateway

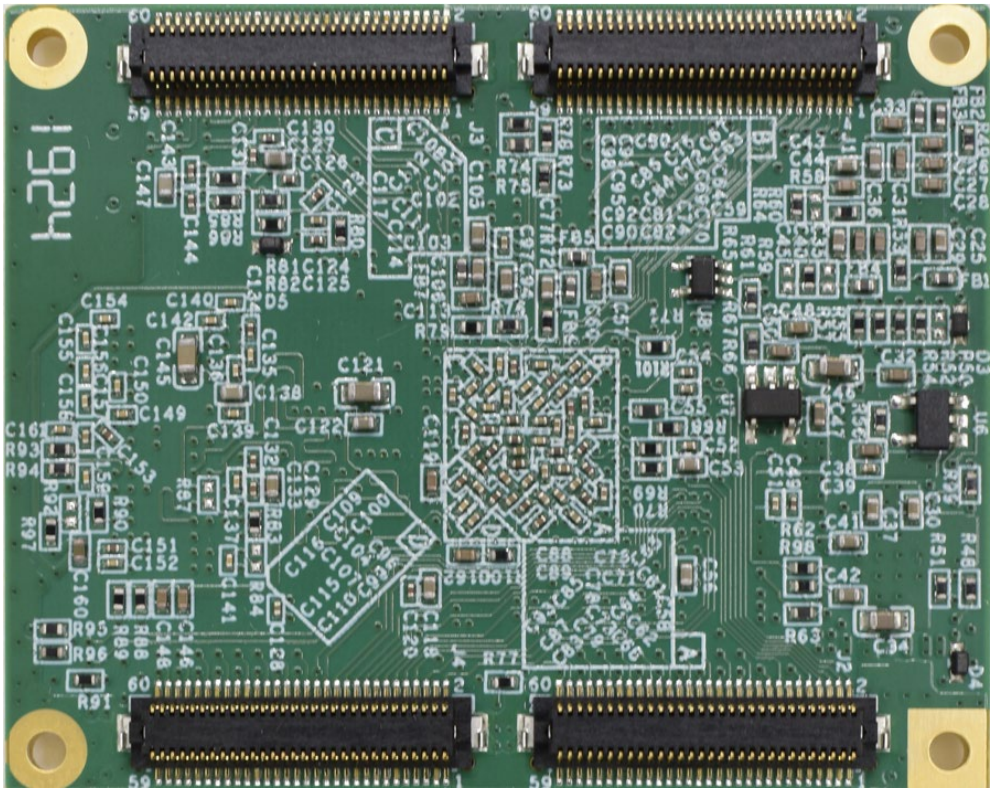
- Human-Machine Interface
- Home Energy Management System
- Smart Energy Information Concentrator
- Smart Industrial Control System
- Electronic POS Equipment
- Medical Equipment
- Printers and 2D Scanners

Note: The peripheral interface characteristics listed above are theoretical quantities. The actual peripheral resources of the SOM-ET-AM62 are subject to the interface description.

2. Features

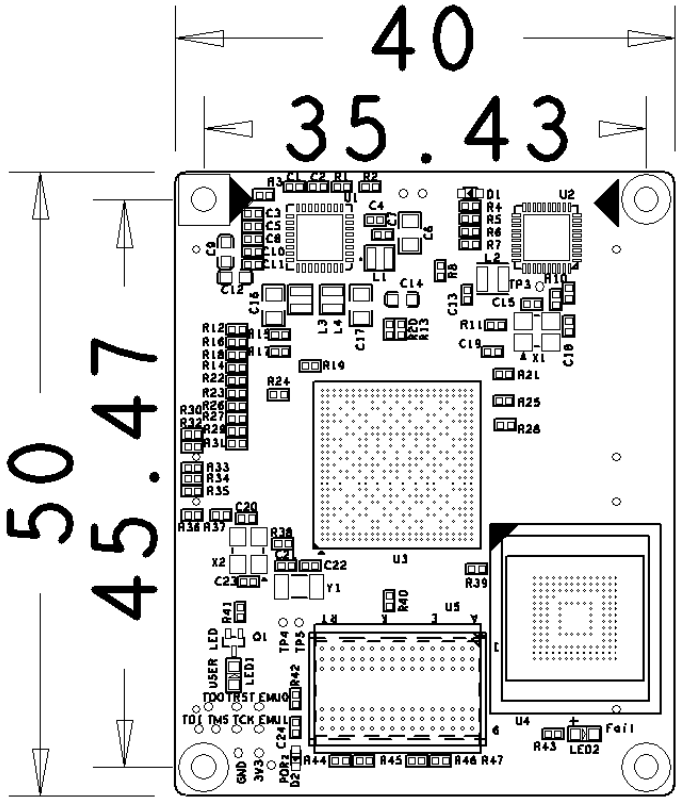


Picture1. Front Functional Features

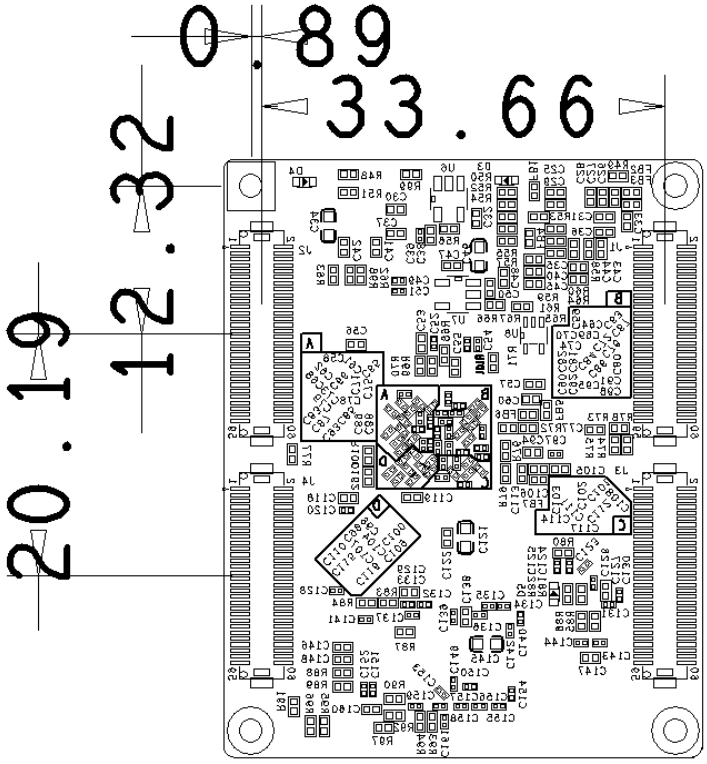


Picture2. Back Functional Features

2.1 Mechanical Dimensions



Picture3. Mechanical Dimensions 1



Picture4. Backside Functional Features 2

2.2 Operating Temperature

Table2.1 Operating Temperature (Junction Temperature)

Specification	M inimum (℃)	Type (℃)	Maximum (℃)
Commercial Grade	0	25	70
Industrial Grade	－40	25	＋85
Storage	－40	25	＋125

2.3 Operating Humidity

Table2.2 Operating Humidity (Junction)

Specification	Minimum Humidity Value (%)	Maximum Humidity Value (%)
Operating Humidity (Non-condensing)	10	90
Storage Humidity	5	95

(Non-condensing)		

2.4 Electrical Parameters

Table2.3 Operating Humidity (Junction)

Specification	Power Consumption
Typical Power Consumption	3.3V/550mA (AM6354)
Maximum Power Consumption	3.3V/1000mA (AM6354)
Recommended Input (Minimum)	3.3V/2A

3. Hardware Description

3.1 System Block Diagram

Table3.1 System Components

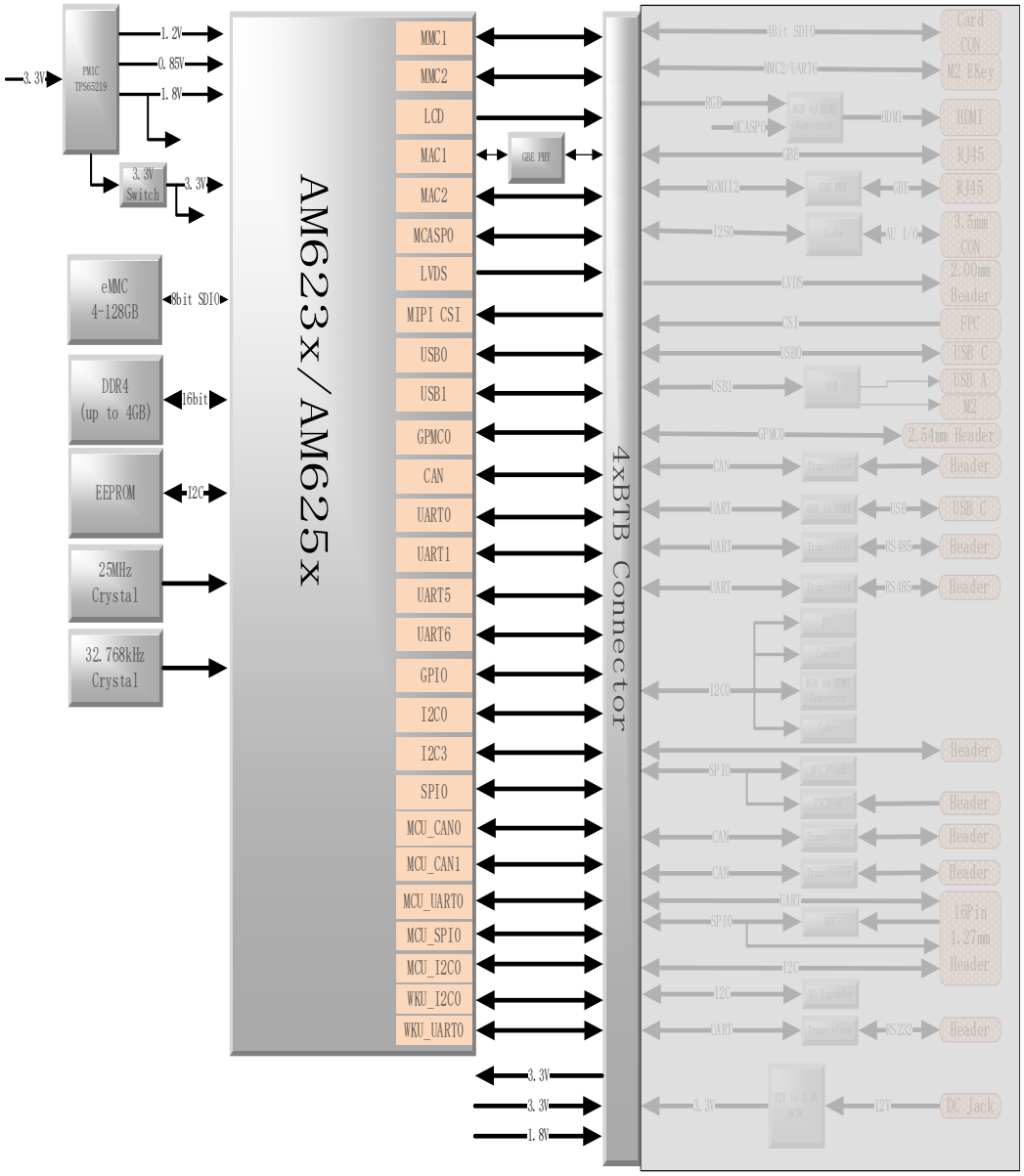
Feature	Details
SOM-ET-AM62	
CPU	Up to 4x ARM Cortex-A53, including: • Up to 1400MHz • 32 KB L1 Instruction Cache • 32 KB L1 Data Cache

	• Single-core ARM Cortec-M4F up to 400MHz • Display Subsystem • 3D Graphics Processing Unit • One Camera Serial Interface • DDR Subsystem
Memory and storage	
DDR SDRAM	• 2GB DDR4 SDRAM (16-bit bus width) • Maximum 4GB support • 1600MHz maximum DDR clock
eMMC	• 8GB eMMC flash memory Default • 8-bits MMC mode • 4~128GB storage option
Expandable flash (MicroSD)	• Runs at 4-bits • Supports system boot from SD card
Network & Wireless	
Ethernet	• 2x 10/100/1000 Mbps Ethernet Controller
Hardware Interface	
I/O connectivity	• 1x 8bit MMC • 1x 4bit MMC • 1x MCASP • 1x GPMC • 1x MAC • 1x GBE • 2x USB OTG • 2x SPI

	• 3x CAN • 6x UART
Display Interfaces	• 1x 16bits RGB LCD • 1x Dual Chennel LVDS
Camera	• 1x MIPI CSI

3.2 Functional Block Diagram

The diagram below is used to describe the internal functional relationship diagram of the EVK-ET-AM62:

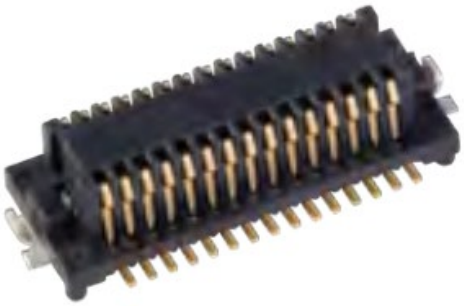


Picture5. Functional Block Diagrams

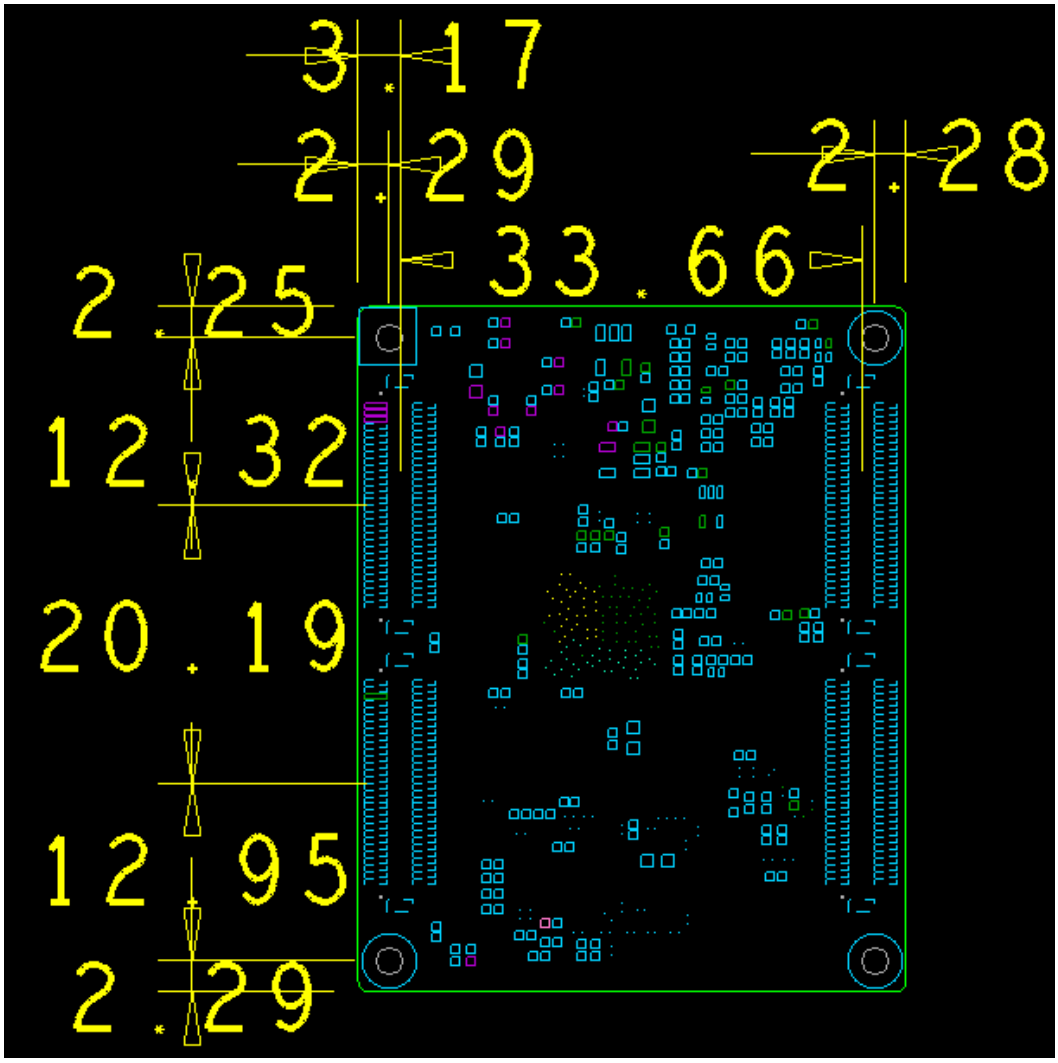
3.3 Connector

The SOM-ET-AM62 core board uses four 60-pin board-to-board connectors to achieve signal output and power supply functions. The connectors are dual-row 0.5mm pitch high-speed signal connectors with a height of 2.15mm. With different mating connectors, a maximum mating height of 4.5mm can be achieved.

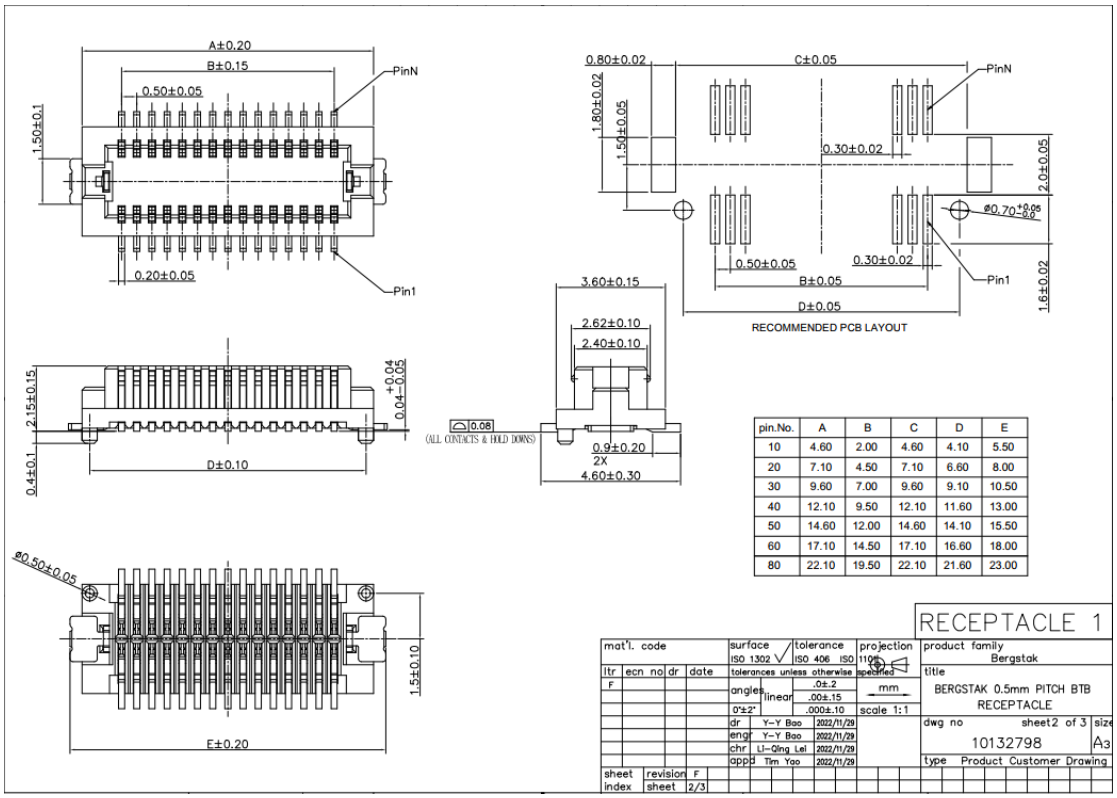
1） Connector outline diagram:



2） The board position is as follows (top view):



3） The specifications of the board-to-board connectors are as follows:



pin.No.	A	B	C	D	E
10	4.60	2.00	4.60	4.10	5.50
20	7.10	4.50	7.10	6.60	8.00
30	9.60	7.00	9.60	9.10	10.50
40	12.10	9.50	12.10	11.60	13.00
50	14.60	12.00	14.60	14.10	15.50
60	17.10	14.50	17.10	16.60	18.00
80	22.10	19.50	22.10	21.60	23.00

4） Connector Pin Definition

In the table below, the signal names are the functional definitions of the SOM-ET-AM62 core module. Other columns are the achievable functional options. If you need to implement the corresponding functions, please contact EMTOP for customization.

J1												
Item	Signal Name	Mux0	Mux1	Mux2	Mux3	Mux4	Mux5	Mux6	Mux7	Mux8	Mux9	Ball State
1	RGMII2_RD3	RGMII2_RD3		AUDIO_EXT_REFCLK0	PR0_PRU0_GPO16	PR0_PRU0_GPI16	PR0_UART0_TXD		GPIO1_6	EQEP2_B		OFF
2	PHY1_LED2	PHY1_LED2										
3	RGMII2_RD2	RGMII2_RD2		MCASP2_AXR0	PR0_PRU0_GPO4	PR0_PRU0_GPI4	PR0_UART0_RXD		GPIO1_5	EQEP2_A		OFF
4	PHY1_LED1	PHY1_LED1										
5	RGMII2_RD1	RGMII2_RD1	RMII2_RXD1	MCASP2_AFSR	PR0_PRU0_GPO3	PR0_PRU0_GPI3	MCASP2_AXR7		GPIO1_4			OFF
6	PHY1_LED0	PHY1_LED0										
7	RGMII2_RD0	RGMII2_RD0	RMII2_RXD0	MCASP2_AXR2	PR0_PRU0_GPO2	PR0_PRU0_GPI2		PR0_UART0_RTSn	GPIO1_3			OFF
8	GND											
9	RGMII2_RXC	RGMII2_RXC	RMII2_REF_CLK	MCASP2_AXR1	PR0_PRU0_GPO1	PR0_PRU0_GPI1	PR0_ECAP0_SYNC_IN		GPIO1_2			OFF
10	PHY1_MDI3N	PHY1_MDI3N										
11	RGMII2_RX_CTL	RGMII2_RX_CTL	RMII2_RX_ER	MCASP2_AXR3	PR0_PRU0_GPO0	PR0_PRU0_GPI0			GPIO1_1			OFF
12	PHY1_MDI3P	PHY1_MDI3P										
13	RGMII2_TX_CTL	RGMII2_TX_CTL	RMII2_TX_EN	MCASP2_AXR4	PR0_PRU1_GPO0	PR0_PRU1_GPI0			GPIO0_87			OFF
14	PHY1_MDI2N	PHY1_MDI2N										
15	RGMII2_TD3	RGMII2_TD3		MCASP2_ACLKX	PR0_PRU1_GPO16	PR0_PRU1_GPI16	PR0_ECAP0_SYNC_OUT	PR0_UART0_CTSn	GPIO1_0	EQEP2_S		OFF
16	PHY1_MDI2P	PHY1_MDI2P										
17	RGMII2_TD2	RGMII2_TD2		MCASP2_AFSX	PR0_PRU1_GPO4	PR0_PRU1_GPI4	PR0_ECAP0_IN_APWM_OUT		GPIO0_91	EQEP2_I		OFF
18	PHY1_MDI1N	PHY1_MDI1N										
19	RGMII2_TD1	RGMII2_TD1	RMII2_TXD1	MCASP2_ACLKR	PR0_PRU1_GPO3	PR0_PRU1_GPI3	MCASP2_AXR8		GPIO0_90			OFF
20	PHY1_MDI1P	PHY1_MDI1P										
21	RGMII2_TD0	RGMII2_TD0	RMII2_TXD0	MCASP2_AXR6	PR0_PRU1_GPO2	PR0_PRU1_GPI2			GPIO0_89			OFF
22	PHY1_MDI0N	PHY1_MDI0N										
23	RGMII2_TXC	RGMII2_TXC	RMII2_CRS_DV	MCASP2_AXR5	PR0_PRU1_GPO1	PR0_PRU1_GPI1			GPIO0_88			OFF
24	PHY1_MDI0P	PHY1_MDI0P										
25	GND											
26	GND											
27	LCD_PCLK	VOUT0_PCLK	GPMC0_A19	PR0_PRU1_GPO19	PR0_PRU1_GPI19	UART2_CTSn	PR0_PRU0_GPO19	PR0_PRU0_GPI19	GPIO0_64	PR0_ECAP0_IN_APWM_OUT		OFF
28	RGMII_MDC											
29	LCD_HSYNC	VOUT0_HSYNC	GPMC0_A16	PR0_PRU1_GPO15	PR0_PRU1_GPI15	UART3_RTSn	PR0_PRU0_GPO6	PR0_PRU0_GPI6	GPIO0_61			OFF
30	RGMII_MDIO											
31	LCD_VSYNC	VOUT0_VSYNC	GPMC0_A18	PR0_PRU1_GPO18	PR0_PRU1_GPI18	UART2_RTSn	PR0_PRU0_GPO18	PR0_PRU0_GPI18	GPIO0_63			OFF
32	LCD_DAT3	VOUT0_DATA3	GPMC0_A3	PR0_PRU1_GPO3	PR0_PRU1_GPI3	UART3_TXD	PR0_PRU0_GPO11	PR0_PRU0_GPI11	GPIO0_48			OFF
33	LCD_DE	VOUT0_DE	GPMC0_A17	PR0_PRU1_GPO17	PR0_PRU1_GPI17	UART3_CTSn	PR0_PRU0_GPO7	PR0_PRU0_GPI7	GPIO0_62			OFF
34	LCD_DAT1	VOUT0_DATA1	GPMC0_A1	PR0_PRU1_GPO1	PR0_PRU1_GPI1	UART2_TXD	PR0_PRU0_GPO9	PR0_PRU0_GPI9	GPIO0_46			OFF
35	LCD_DAT0	VOUT0_DATA0	GPMC0_A0	PR0_PRU1_GPO0	PR0_PRU1_GPI0	UART2_RXD	PR0_PRU0_GPO8	PR0_PRU0_GPI8	GPIO0_45			OFF

36	LCD_DAT13	VOUT0_DATA13	GPMC0_A13	PR0_PRU1_GPO12	PR0_PRU1_GPI12	UART5_CTSn	PR0_PRU0_GPO3	PR0_PRU0_GPI3	GPIO0_58			OFF
37	LCD_DAT2	VOUT0_DATA2	GPMC0_A2	PR0_PRU1_GPO2	PR0_PRU1_GPI2	UART3_RXD	PR0_PRU0_GPO10	PR0_PRU0_GPI10	GPIO0_47			OFF
38	LCD_DAT5	VOUT0_DATA5	GPMC0_A5	PR0_PRU1_GPO5	PR0_PRU1_GPI5	UART4_TXD	PR0_PRU0_GPO13	PR0_PRU0_GPI13	GPIO0_50			OFF
39	LCD_DAT6	VOUT0_DATA6	GPMC0_A6	PR0_PRU1_GPO6	PR0_PRU1_GPI6	UART5_RXD	PR0_PRU0_GPO14	PR0_PRU0_GPI14	GPIO0_51			OFF
40	LCD_DAT12	VOUT0_DATA12	GPMC0_A12	PR0_PRU1_GPO11	PR0_PRU1_GPI11	UART5_RTSn	PR0_PRU0_GPO2	PR0_PRU0_GPI2	GPIO0_57			OFF
41	LCD_DAT8	VOUT0_DATA8	GPMC0_A8	PR0_PRU1_GPO16	PR0_PRU1_GPI16	UART6_RXD	PR0_PRU0_GPO17	PR0_PRU0_GPI17	GPIO0_53			OFF
42	LCD_DAT7	VOUT0_DATA7	GPMC0_A7	PR0_PRU1_GPO7	PR0_PRU1_GPI7	UART5_TXD	PR0_PRU0_GPO15	PR0_PRU0_GPI15	GPIO0_52			OFF
43	LCD_DAT15	VOUT0_DATA15	GPMC0_A15	PR0_PRU1_GPO14	PR0_PRU1_GPI14	UART4_CTSn	PR0_PRU0_GPO5	PR0_PRU0_GPI5	GPIO0_60			OFF
44	LCD_DAT4	VOUT0_DATA4	GPMC0_A4	PR0_PRU1_GPO4	PR0_PRU1_GPI4	UART4_RXD	PR0_PRU0_GPO12	PR0_PRU0_GPI12	GPIO0_49			OFF
45	HFOSC0_CLKOUT_32K	WKUP_CLKOUT0							MCU_GPIO0_23			OFF
46	LCD_DAT9	VOUT0_DATA9	GPMC0_A9	PR0_PRU1_GPO8	PR0_PRU1_GPI8	UART6_TXD	PR0_PRU0_GPO16	PR0_PRU0_GPI16	GPIO0_54			OFF
47	UART0_RTS	UART0_RTSn	SPI0_CS3	I2C3_SDA	UART2_TXD	TIMER_IO7	AUDIO_EXT_REFCLK1	PR0_ECAP0_IN_APWM_OUT	GPIO1_23	MCASP2_ACLKX	MMC2_SDWP	OFF
48	LCD_DAT14	VOUT0_DATA14	GPMC0_A14	PR0_PRU1_GPO13	PR0_PRU1_GPI13	UART4_RTSn	PR0_PRU0_GPO4	PR0_PRU0_GPI4	GPIO0_59			OFF
49	UART0_CTS	UART0_CTSn	SPI0_CS2	I2C3_SCL	UART2_RXD	TIMER_IO6	AUDIO_EXT_REFCLK0	PR0_ECAP0_SYNC_OUT	GPIO1_22	MCASP2_AFSX	MMC2_SDCD	OFF
50	LCD_DAT11	VOUT0_DATA11	GPMC0_A11	PR0_PRU1_GPO10	PR0_PRU1_GPI10	UART6_CTSn	PR0_PRU0_GPO1	PR0_PRU0_GPI1	GPIO0_56			OFF
51	EXP_REFCLK1	EXT_REFCLK1	SYNC1_OUT	SPI2_CS3	SYSCLKOUT0	TIMER_IO4	CLKOUT0	CP_GEMAC_CPTS0_RFT_CLK	GPIO1_30	ECAP0_IN_APWM_OUT		OFF
52	LCD_DAT10	VOUT0_DATA10	GPMC0_A10	PR0_PRU1_GPO9	PR0_PRU1_GPI9	UART6_RTSn	PR0_PRU0_GPO0	PR0_PRU0_GPI0	GPIO0_55			OFF
53	MCAN0_RXD	MCAN0_RX	UART5_TXD	TIMER_IO3	SYNC3_OUT	UART1_Rin	EQEP2_S	PR0_UART0_TXD	GPIO1_25	MCASP2_AXR1	EHRPWM_TZn_IN4	OFF
54	WKUP_I2C0_SCL	WKUP_I2C0_SCL							MCU_GPIO0_19			OFF
55	MCAN0_TXD	MCAN0_TX	UART5_RXD	TIMER_IO2	SYNC2_OUT	UART1_DTRn	EQEP2_I	PR0_UART0_RXD	GPIO1_24	MCASP2_AXR0	EHRPWM_TZn_IN3	OFF
56	WKUP_I2C0_SDA	WKUP_I2C0_SDA							MCU_GPIO0_20			OFF
57	UART0_RXD	UART0_RXD	ECAP1_IN_APWM_OUT	SPI2_D0	EHRPWM2_A				GPIO1_20			OFF
58	MCU_I2C0_SCL	MCU_I2C0_SCL							MCU_GPIO0_17			OFF
59	UART0_TXD	UART0_TXD	ECAP2_IN_APWM_OUT	SPI2_D1	EHRPWM2_B				GPIO1_21			OFF
60	MCU_I2C0_SDA	MCU_I2C0_SDA							MCU_GPIO0_18			OFF

J2

Item	Signal Name	Mux0	Mux1	Mux2	Mux3	Mux4	Mux5	Mux6	Mux7	Mux8	Mux9	Ball State
1	VDD3V3_MAIN											
2	GPMC0_WAIT0	GPMC0_WAIT0		MCASP1_AFSX		PR0_PRU0_GPO14	PR0_PRU0_GPI14	TRC_DATA12	GPIO0_37			OFF
3	VDD3V3_MAIN											
4	GPMC0_WAIT1	GPMC0_WAIT1	VOUT0_EXTPCLKIN	GPMC0_A21	UART6_RXD				GPIO0_38	EQEP2_I		OFF
5	VDD3V3_MAIN											
6	GPMC0_BE0E_CLE	GPMC0_BE0n_CLE		MCASP1_ACLKX		PR0_PRU0_GPO12	PR0_PRU0_GPI12	TRC_DATA10	GPIO0_35			OFF
7	NC											
8	GPMC0_OEN_REN	GPMC0_OEn_Ren		MCASP1_AXR1		PR0_PRU0_GPO10	PR0_PRU0_GPI10	TRC_DATA8	GPIO0_33			OFF
9	I2C1_SDA	I2C1_SDA	UART1_TXD	TIMER_IO1	SPI2_CLK	EHRPWM0_SYNCO			GPIO1_29	EHRPWM2_B	MMC2_SDWP	OFF

10	GPMC0_WEN	GPMC0_Wen		MCASP1_AXR0		PR0_PRU0_GPO11	PR0_PRU0_GPI11	TRC_DATA9	GPIO0_34			OFF
11	I2C1_SCL	I2C1_SCL	UART1_RXD	TIMER_IO0	SPI2_CS1	EHRPWM0_SYNCI			GPIO1_28	EHRPWM2_A	MMC2_SDCD	OFF
12	GPMC0_DIR	GPMC0_DIR		PR0_ECAP0_IN_APWM_OUT	MCASP2_AXR13	PR0_PRU0_GPO16	PR0_PRU0_GPI16	TRC_DATA14	GPIO0_40	EQEP2_S		OFF
13	I2C0_SDA	I2C0_SDA	PR0_IEP0_EDIO_DATA_IN_OUT31	SPI2_CS2	TIMER_IO5	UART1_DSRn	EQEP2_B	EHRPWM_SOCB	GPIO1_27	ECAP2_IN_APWM_OUT		OFF
14	GPMC0_BE1E	GPMC0_BE1n			MCASP2_AXR12	PR0_PRU0_GPO13	PR0_PRU0_GPI13	TRC_DATA11	GPIO0_36			OFF
15	I2C0_SCL	I2C0_SCL	PR0_IEP0_EDIO_DATA_IN_OUT30	SYNC0_OUT	OBSCLK0	UART1_DCDn	EQEP2_A	EHRPWM_SOCA	GPIO1_26	ECAP1_IN_APWM_OUT	SPI2_CS0	OFF
16	GPMC0_WPN	GPMC0_WPn	AUDIO_EXT_REFCLK1	GPMC0_A22	UART6_TXD	PR0_PRU0_GPO15	PR0_PRU0_GPI15	TRC_DATA13	GPIO0_39			OFF
17	SPI0_CS1	SPI0_CS1	CP_GEMAC_CPTS0_TS_COMP	EHRPWM0_B	ECAP0_IN_APWM_OUT				GPIO1_16		EHRPWM_TZn_IN5	OFF
18	GPMC0_ADVN_ALE	GPMC0_ADVn_ALE	MCASP1_AXR2	PR0_PRU0_GPO9	PR0_PRU0_GPI9	TRC_DATA7			GPIO0_32			OFF
19	SPI0_CS0	SPI0_CS0		EHRPWM0_A				PR0_ECAP0_SYNC_IN	GPIO1_15			OFF
20	GND											
21	SPI0_D1	SPI0_D1	CP_GEMAC_CPTS0_HW2TSPUSH	EHRPWM_TZn_IN0					GPIO1_19			OFF
22	GPMC0_CLK	GPMC0_CLK		MCASP1_AXR3	GPMC0_FCLK_MUX	PR0_PRU0_GPO8	PR0_PRU0_GPI8	TRC_DATA6	GPIO0_31			OFF
23	SPI0_D0	SPI0_D0	CP_GEMAC_CPTS0_HW1TSPUSH	EHRPWM1_B					GPIO1_18			OFF
24	GND											
25	SPI0_CLK	SPI0_CLK	CP_GEMAC_CPTS0_TS_SYNC	EHRPWM1_A					GPIO1_17			OFF
26	GPMC0_AD15	GPMC0_AD15	VOUT0_DATA23	UART5_TXD	MCASP2_ACLKR	PR0_PRU0_GPO3	PR0_PRU0_GPI3	TRC_DATA19	GPIO0_30	UART2_RTSn		OFF
27	MCU_UART0_RTS	MCU_UART0_RTSn	MCU_TIMER_IO1		MCU_SPI1_D1				MCU_GPIO0_8			OFF
28	GPMC0_AD14	GPMC0_AD14	VOUT0_DATA22	UART5_RXD	MCASP2_AFSR	PR0_PRU0_GPO2	PR0_PRU0_GPI2	TRC_DATA20	GPIO0_29	UART2_CTSn		OFF
29	MCU_UART0_CTS	MCU_UART0_CTSn	MCU_TIMER_IO0		MCU_SPI1_D0				MCU_GPIO0_7			OFF
30	GPMC0_AD10	GPMC0_AD10	VOUT0_DATA18	UART3_RXD	MCASP2_AXR2	PR0_PRU1_GPO2	PR0_PRU1_GPI2		GPIO0_25	OBSCLK0		OFF
31	MCU_UART0_TXD	MCU_UART0_TXD							MCU_GPIO0_6			OFF
32	GPMC0_AD4	GPMC0_AD4	PR0_PRU1_GPO12	PR0_PRU1_GPI12	MCASP2_AXR8	PR0_PRU0_GPO4	PR0_PRU0_GPI4	TRC_DATA2	GPIO0_19			OFF
33	MCU_UART0_RXD	MCU_UART0_RXD							MCU_GPIO0_5			OFF
34	GPMC0_AD0	GPMC0_AD0	PR0_PRU1_GPO8	PR0_PRU1_GPI8	MCASP2_AXR4	PR0_PRU0_GPO0	PR0_PRU0_GPI0	TRC_CLK	GPIO0_15			OFF
35	GND											
36	GPMC0_AD3	GPMC0_AD3	PR0_PRU1_GPO11	PR0_PRU1_GPI11	MCASP2_AXR7	PR0_PRU0_GPO3	PR0_PRU0_GPI3	TRC_DATA1	GPIO0_18			OFF
37	RESETSTATz	RESETSTATz										LOW
38	GPMC0_AD2	GPMC0_AD2	PR0_PRU1_GPO10	PR0_PRU1_GPI10	MCASP2_AXR6	PR0_PRU0_GPO2	PR0_PRU0_GPI2	TRC_DATA0	GPIO0_17			OFF
39	RESET_REQz	RESET_REQz										OFF
40	GPMC0_AD8	GPMC0_AD8	VOUT0_DATA16	UART2_RXD	MCASP2_AXR0	PR0_PRU1_GPO0	PR0_PRU1_GPI0		GPIO0_23			OFF
41	PORz_OUT	PORz_OUT										LOW
42	GND											
43	MCU_RESETz	MCU_RESETz										OFF
44	GPMC0_AD9	GPMC0_AD9	VOUT0_DATA17	UART2_TXD	MCASP2_AXR1	PR0_PRU1_GPO1	PR0_PRU1_GPI1		GPIO0_24			OFF
45	MCU_RESETSTATz	MCU_RESETSTATz							MCU_GPIO0_21			LOW
46	GPMC0_AD13	GPMC0_AD13	VOUT0_DATA21	UART4_TXD	MCASP2_ACLKX	PR0_PRU0_GPO1	PR0_PRU0_GPI1	TRC_DATA21	GPIO0_28			OFF
47	PMIC_GPO1											
48	GPMC0_AD12	GPMC0_AD12	VOUT0_DATA20	UART4_RXD	MCASP2_AFSX	PR0_PRU0_GPO0	PR0_PRU0_GPI0	TRC_DATA22	GPIO0_27			OFF

49	PMIC_PBn											
50	GPMC0_AD5	GPMC0_AD5	PR0_PRU1_GPO13	PR0_PRU1_GPI13	MCASP2_AXR9	PR0_PRU0_GPO5	PR0_PRU0_GPI5	TRC_DATA3	GPIO0_20			OFF
51	GND											
52	GPMC0_AD7	GPMC0_AD7	PR0_PRU1_GPO15	PR0_PRU1_GPI15	MCASP2_AXR11	PR0_PRU0_GPO7	PR0_PRU0_GPI7	TRC_DATA5	GPIO0_22			OFF
53	GPMC0_CSN3	GPMC0_CSn3	I2C2_SDA	GPMC0_A20	UART4_TXD	MCASP1_AXR5		TRC_DATA18	GPIO0_44	MCASP1_ACLKR		OFF
54	GPMC0_AD11	GPMC0_AD11	VOUT0_DATA19	UART3_TXD	MCASP2_AXR3	PR0_PRU1_GPO3	PR0_PRU1_GPI3	TRC_DATA23	GPIO0_26			OFF
55	GPMC0_CSN2	GPMC0_CSn2	I2C2_SCL	MCASP1_AXR4	UART4_RXD	PR0_PRU0_GPO19	PR0_PRU0_GPI19	TRC_DATA17	GPIO0_43	MCASP1_AFSR		OFF
56	GPMC0_AD1	GPMC0_AD1	PR0_PRU1_GPO9	PR0_PRU1_GPI9	MCASP2_AXR5	PR0_PRU0_GPO1	PR0_PRU0_GPI1	TRC_CTL	GPIO0_16			OFF
57	GPMC0_CSN1	GPMC0_CSn1	PR0_PRU1_GPO16	PR0_PRU1_GPI16	MCASP2_AXR15	PR0_PRU0_GPO18	PR0_PRU0_GPI18	TRC_DATA16	GPIO0_42			OFF
58	GPMC0_AD6	GPMC0_AD6	PR0_PRU1_GPO14	PR0_PRU1_GPI14	MCASP2_AXR10	PR0_PRU0_GPO6	PR0_PRU0_GPI6	TRC_DATA4	GPIO0_21			OFF
59	GPMC0_CSN0	GPMC0_CSn0			MCASP2_AXR14	PR0_PRU0_GPO17	PR0_PRU0_GPI17	TRC_DATA15	GPIO0_41			OFF
60	GND											

J3

Item	Signal Name	Mux0	Mux1	Mux2	Mux3	Mux4	Mux5	Mux6	Mux7	Mux8	Mux9	Ball State
1	GND											
2	GND											
3	OLDI0_CLK1P	OLDI0_CLK1P										
4	CSI0_RXP3	CSI0_RXP3										
5	OLDI0_CLK1N	OLDI0_CLK1N										
6	CSI0_RXN3	CSI0_RXN3										
7	GND											
8	GND											
9	OLDI0_CLK0N	OLDI0_CLK0N										
10	CSI0_RXN2	CSI0_RXN2										
11	OLDI0_CLK0P	OLDI0_CLK0P										
12	CSI0_RXP2	CSI0_RXP2										
13	GND											
14	GND											
15	OLDI0_A0P	OLDI0_A0P										
16	CSI0_RXP1	CSI0_RXP1										
17	OLDI0_A0N	OLDI0_A0N										
18	CSI0_RXN1	CSI0_RXN1										
19	GND											
20	GND											
21	OLDI0_A1P	OLDI0_A1P										
22	CSI0_RXN0	CSI0_RXN0										

23	OLDI0_A1N	OLDI0_A1N										
24	CSI0_RXP0	CSI0_RXP0										
25	GND											
26	GND											
27	OLDI0_A2P	OLDI0_A2P										
28	CSI0_RXCLKN	CSI0_RXCLKN										
29	OLDI0_A2N	OLDI0_A2N										
30	CSI0_RXCLKP	CSI0_RXCLKP										
31	GND											
32	GND											
33	OLDI0_A3P	OLDI0_A3P										
34	USB1_DM	USB1_DM										
35	OLDI0_A3N	OLDI0_A3N										
36	USB1_DP	USB1_DP										
37	GND											
38	GND											
39	OLDI0_A4P	OLDI0_A4P										
40	USB0_DM	USB0_DM										
41	OLDI0_A4N	OLDI0_A4N										
42	USB0_DP	USB0_DP										
43	GND											
44	GND											
45	OLDI0_A5N	OLDI0_A5N										
46	GND											
47	OLDI0_A5P	OLDI0_A5P										
48	GND											
49	GND											
50	USB0_VBUS	USB0_VBUS										
51	OLDI0_A6P	OLDI0_A6P										
52	WKUP_UART0_CTS	WKUP_UART0_CTSn	WKUP_TIMER_IO0		MCU_SPI1_CS0				MCU_GPIO0_11			OFF
53	OLDI0_A6N	OLDI0_A6N										
54	WKUP_UART0_RTS	WKUP_UART0_RTSn	WKUP_TIMER_IO1		MCU_SPI1_CLK				MCU_GPIO0_12			OFF
55	GND											
56	WKUP_UART0_TXD	WKUP_UART0_TXD		MCU_SPI1_CS2					MCU_GPIO0_10			OFF
57	OLDI0_A7P	OLDI0_A7P										
58	WKUP_UART0_RXD	WKUP_UART0_RXD		MCU_SPI0_CS2					MCU_GPIO0_9			OFF
59	OLDI0_A7N	OLDI0_A7N										
60	USB0_DRVVBUS								GPIO1_50			OFF

J4												
Item	Signal Name	Mux0	Mux1	Mux2	Mux3	Mux4	Mux5	Mux6	Mux7	Mux8	Mux9	Ball State
1	PMIC_GPO								GPIO0_0			OFF
2	OSPI0_CLK	OSPI0_CLK										
3	GND											
4	GND											
5	VDD3V3											
6	OSPI0_D1	OSPI0_D1							GPIO0_4			OFF
7	VDD_OSPI											
8	OSPI0_D0	OSPI0_D0							GPIO0_3			OFF
9	VDD_MMC2											
10	OSPI0_D2	OSPI0_D2							GPIO0_5			OFF
11	VDD1V8											
12	OSPI0_D3	OSPI0_D3							GPIO0_6			OFF
13	GND											
14	OSPI0_LBCLKO	OSPI0_LBCLKO					UART5_RTSn		GPIO0_1			OFF
15	OSPI0_CSN3	OSPI0_CSn3	OSPI0_RESET_OUT0	OSPI0_ECC_FAIL	MCASP1_ACLKR	MCASP1_AXR3	UART5_TXD		GPIO0_14			OFF
16	OSPI0_D6	OSPI0_D6	SPI1_D0	MCASP1_ACLKX	UART6_RTSn				GPIO0_9			OFF
17	OSPI0_CSN2	OSPI0_CSn2	SPI1_CS1	OSPI0_RESET_OUT1	MCASP1_AFSR	MCASP1_AXR2	UART5_RXD		GPIO0_13			OFF
18	OSPI0_DQS	OSPI0_DQS					UART5_CTSn		GPIO0_2			OFF
19	MCASP0_ACLKX	MCASP0_ACLKX	SPI2_CS1	ECAP2_IN_APWM_OUT					GPIO1_11	EQEP1_A		OFF
20	OSPI0_D4	OSPI0_D4	SPI1_CS0	MCASP1_AXR1	UART6_RXD				GPIO0_7			OFF
21	MCASP0_AFSR	MCASP0_AFSR	SPI2_CS0	UART1_RXD				EHRPWM0_A	GPIO1_13	EQEP1_S		OFF
22	OSPI0_D5	OSPI0_D5	SPI1_CLK	MCASP1_AXR0	UART6_TXD				GPIO0_8			OFF
23	MCASP0_AFSX	MCASP0_AFSX	SPI2_CS3	AUDIO_EXT_REFCLK1					GPIO1_12	EQEP1_B		OFF
24	OSPI0_D7	OSPI0_D7	SPI1_D1	MCASP1_AFSX	UART6_CTSn				GPIO0_10			OFF
25	MCASP0_AXR0	MCASP0_AXR0	PR0_ECAP0_IN_APWM_OUT	AUDIO_EXT_REFCLK0			PR0_UART0_TXD	EHRPWM1_B	GPIO1_10	EQEP0_I		OFF
26	OSPI0_CSN0	OSPI0_CSn0							GPIO0_11			OFF
27	MCASP0_AXR2	MCASP0_AXR2	SPI2_D1	UART1_RTSn	UART6_TXD	PR0_IEP0_EDIO_DATA_IN_OUT29	ECAP2_IN_APWM_OUT	PR0_UART0_TXD	GPIO1_8	EQEP0_B		OFF
28	SYS_nLED											
29	MCASP0_AXR3	MCASP0_AXR3	SPI2_D0	UART1_CTSn	UART6_RXD	PR0_IEP0_EDIO_DATA_IN_OUT28	ECAP1_IN_APWM_OUT	PR0_UART0_RXD	GPIO1_7			OFF
30	MCU_MCAN0_RX	MCU_MCAN0_RX	MCU_TIMER_IO0	MCU_SPI1_CS3					MCU_GPIO0_14			OFF
31	MCASP0_ACLKR	MCASP0_ACLKR	SPI2_CLK	UART1_TXD				EHRPWM0_B	GPIO1_14	EQEP1_I		OFF
32	MCU_MCAN0_TX	MCU_MCAN0_TX	WKUP_TIMER_IO0	MCU_SPI0_CS3					MCU_GPIO0_13			OFF
33	MCASP0_AXR1	MCASP0_AXR1	SPI2_CS2	ECAP1_IN_APWM_OUT	PR0_UART0_RXD			EHRPWM1_A	GPIO1_9	EQEP0_S		OFF
34	MCU_MCAN1_RX	MCU_MCAN1_RX	MCU_TIMER_IO3	MCU_SPI0_CS2	MCU_SPI1_CS2	MCU_SPI1_CLK			MCU_GPIO0_16			OFF

35	GND											
36	MCU_MCAN1_TX	MCU_MCAN1_TX	MCU_TIMER_IO2		MCU_SPI1_CS1	MCU_EXT_REFCLK0			MCU_GPIO0_15			OFF
37	MMC2_SDCD	MMC2_SDCD	MCASP1_ACLKX		UART4_RXD				GPIO0_71			OFF
38	MCU_SPI0_D1	MCU_SPI0_D1							MCU_GPIO0_4			OFF
39	MMC2_SDWP	MMC2_SDWP	MCASP1_AFSX		UART4_TXD				GPIO0_72			OFF
40	MCU_SPI0_D0	MCU_SPI0_D0							MCU_GPIO0_3			OFF
41	MMC2_CMD	MMC2_CMD	MCASP1_AFSR	MCASP1_AXR4	UART6_TXD				GPIO0_70			OFF
42	MCU_SPI0_CS0	MCU_SPI0_CS0				WKUP_TIMER_IO1			MCU_GPIO0_0			OFF
43	MMC2_DAT1	MMC2_DAT1	MCASP1_AXR1						GPIO0_67			OFF
44	MCU_SPI0_CS1	MCU_SPI0_CS1	MCU_OBSCLK0	MCU_SYSCLKOUT0	MCU_EXT_REFCLK0	MCU_TIMER_IO1			MCU_GPIO0_1			OFF
45	MMC2_DAT0	MMC2_DAT0	MCASP1_AXR0						GPIO0_68			OFF
46	MCU_SPI0_CLK	MCU_SPI0_CLK							MCU_GPIO0_2			OFF
47	MMC2_DAT2	MMC2_DAT2	MCASP1_AXR2		UART5_TXD				GPIO0_66			OFF
48	GND											
49	MMC2_DAT3	MMC2_DAT3	MCASP1_AXR3		UART5_RXD				GPIO0_65			OFF
50	MMC1_SDCD	MMC1_SDCD	UART6_RXD	TIMER_IO6	UART3_RTSn				GPIO1_48			OFF
51	MMC2_CLK	MMC2_CLK	MCASP1_ACLKR	MCASP1_AXR5	UART6_RXD				GPIO0_69			OFF
52	MMC1_SDWP	MMC1_SDWP	UART6_TXD	TIMER_IO7	UART3_CTSn				GPIO1_49			OFF
53	GND											
54	MMC1_DAT2	MMC1_DAT2	CP_GEMAC_CPTS0_TS_SYNC	TIMER_IO1	UART2_TXD				GPIO1_43			OFF
55	MMC1_CLK	MMC1_CLK		TIMER_IO4	UART3_RXD				GPIO1_46			OFF
56	MMC1_DAT3	MMC1_DAT3	CP_GEMAC_CPTS0_TS_COMP	TIMER_IO0	UART2_RXD				GPIO1_42			OFF
57	MMC1_CMD	MMC1_CMD		TIMER_IO5	UART3_TXD				GPIO1_47			OFF
58	MMC1_DAT0	MMC1_DAT0	CP_GEMAC_CPTS0_HW2TSPUSH	TIMER_IO3	UART2_CTSn	ECAP2_IN_APWM_OUT			GPIO1_45			OFF
59	VDDSHV_SDIO											
60	MMC1_DAT1	MMC1_DAT1	CP_GEMAC_CPTS0_HW1TSPUSH	TIMER_IO2	UART2_RTSn	ECAP1_IN_APWM_OUT			GPIO1_44			OFF

4. Interface Description

This chapter introduces some recommended designs for the peripheral interfaces provided by the SOM-ET-AM62. Users can refer to this chapter for baseboard design.

Note that the circuits introduced in this chapter are only for demo indication or design guidance and are not complete functional designs. Baseboard design engineers need to select appropriate peripheral chips and auxiliary components for functional design based on the application scenarios and performance requirements of the device.

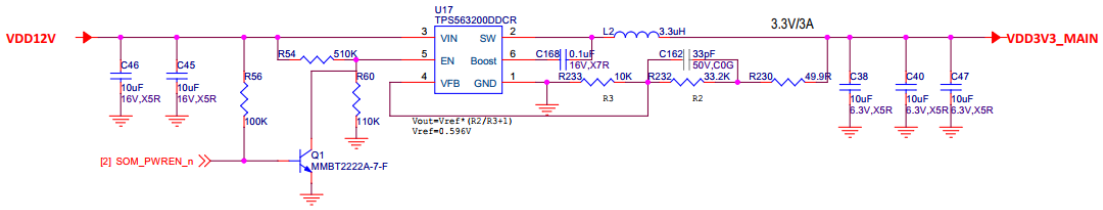
4.1 System Power Supply

Note that this core board uses a 3.3V power supply, not a 5V input. Since the core board may supply power to some peripherals or peripheral IOs on the baseboard, it is recommended that the power supply capability be 3.3V/2.5A or above to ensure the stable operation of the core board.

If the system requires power management or peripheral management, it is recommended to supply power to the core board separately to ensure flexible control of the system power.

The EVK-ET-AM62 uses the TPS563200 chip to supply power to the core board separately. The circuit is shown in the figure below. Note that the SOM_PWREN_N signal is used to detect the insertion of the core board. When the core board is inserted, this signal is grounded, enabling the 3.3V power supply to the core board. When the core board is removed, this signal is left floating, and the power supply to the core board is turned off. If not used, or by removing R56 and Q1, the power supply to the core board is enabled directly upon power-up.

The core board power supply circuit is as follows:



4.2 Reset and Control

1、 The SOM-ET-AM62 has multiple reset sources. All reset pins have been properly designed on the core board. Unused reset pins can be left floating.

2、 During reset, J2.39 can be directly connected to the reset input source, and pulling J1.39 low can achieve the reset function;

3、 J2.49 is the PMIC's button pin, which can achieve PMIC interrupt and hardware reset functions. Providing a long-period low level to this pin will cause the PMIC to reset, thereby causing the entire system to hardware reset.

4、 The J2.47 pin is the PMIC's IO output, which is enabled by software control. If the customer wishes to control the baseboard power, this pin can be directly used as the control pin for the baseboard power.

4.3 Boot Selection

1、 The SOM-ET-AM62 is already configured with the necessary boot configuration circuit, defaulting to boot from eMMC. If you need to change the boot device to boot from the baseboard SD card, you need to pull the GPMC_AD3 pin low when powering on the SOM-ET-AM62 core board. Once the SOM-ET-AM62 is powered on, you can release GPMC_AD3 for normal use.

2、 Since GPMC0~GPMC15, a total of 16 lines, are used as boot configuration pins during power-up, when peripherals need to configure these pins for pull-up or pull-down, please refer to the following table. The external circuit should not change the level of the relevant pins during power-up to avoid affecting the boot process.

Signal	Pull-up/Pull-down	Level Requirement
GPMC_AD0	1K Pull-up	1
GPMC_AD1	1K Pull-up	1
GPMC_AD2	100K Pull-down	0

GPMC_AD3	1K Pull-up	1
GPMC_AD4	100K Pull-down	0
GPMC_AD5	100K Pull-down	0
GPMC_AD6	1K Pull-up	1
GPMC_AD7	100K Pull-down	0
GPMC_AD8	100K Pull-down	0
GPMC_AD9	1K Pull-up	1
GPMC_AD10	100K Pull-down	0
GPMC_AD11	100K Pull-down	0
GPMC_AD12	100K Pull-down	0
GPMC_AD13	100K Pull-down	0
GPMC_AD14	Reserved	Reserved
GPMC_AD15	Reserved	Reserved

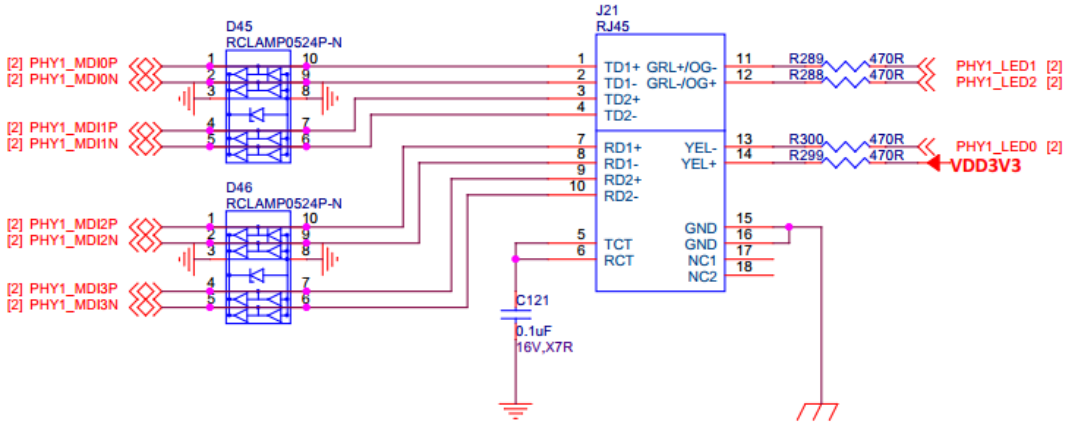
4.4 Network

The SOM-ET-AM62 provides up to 2 MACs, which can offer two gigabit Ethernet ports. Among them, MAC1 has already been designed with a PHY chip on the SOM-ET-AM62, fixed for network functionality. Customers only need to add an RJ45 connector on the baseboard. Therefore, pins 28 and 30 of the BTB connector J1 can only be used for

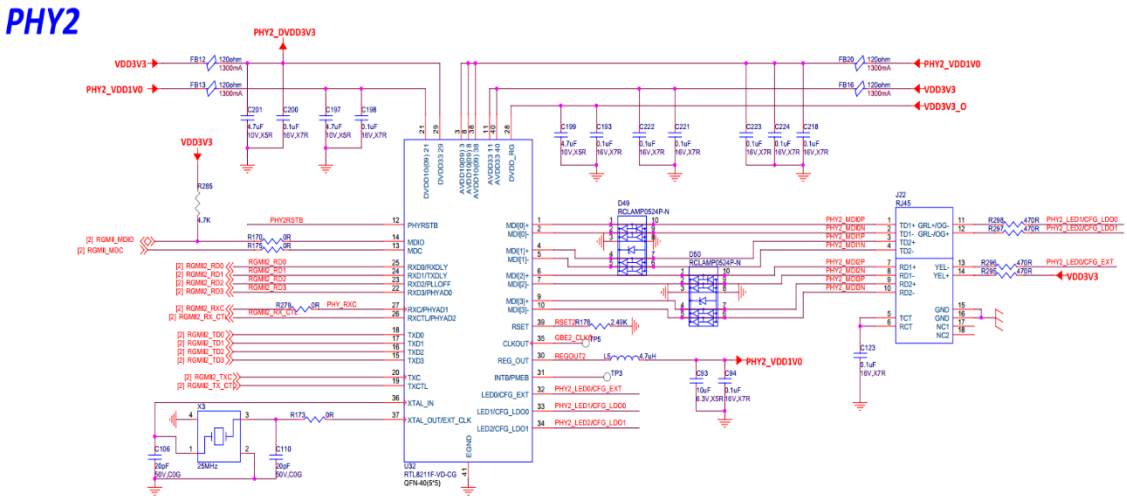
MDIO functionality and cannot be repurposed for other functions such as GPIO.

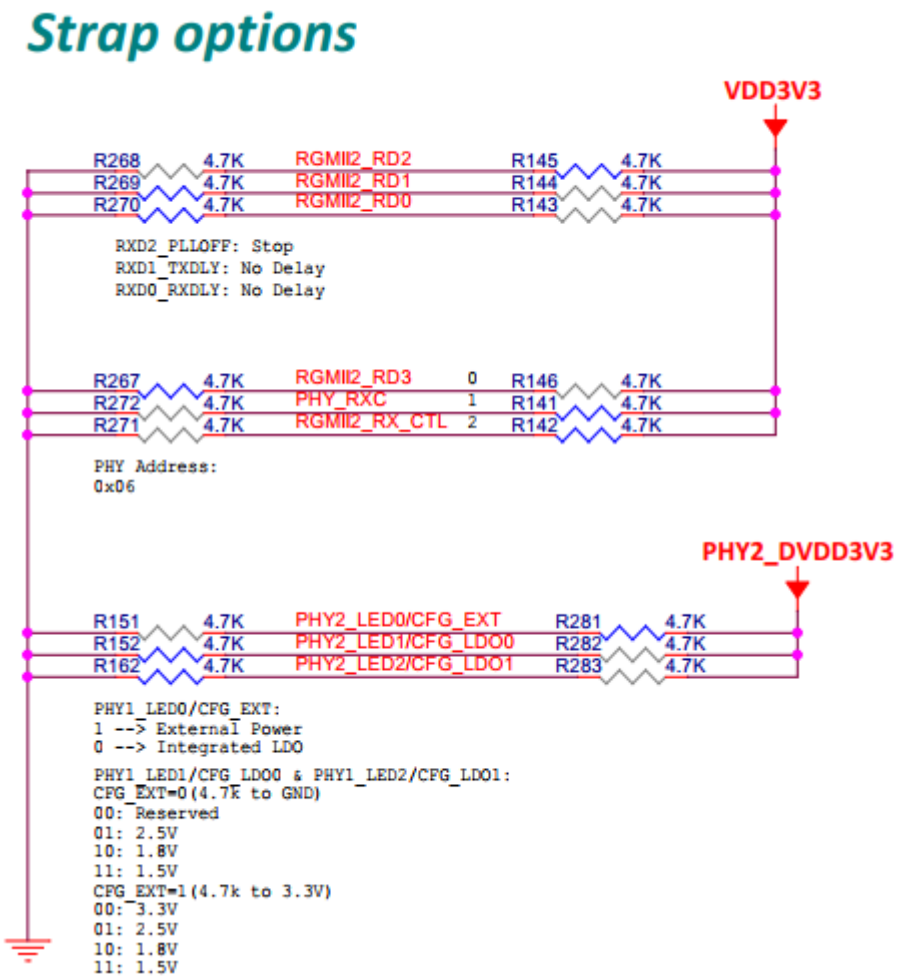
MAC2 is directly connected to the baseboard. Customers can design the PHY on the baseboard to implement the second gigabit network function. If the customer does not need the second gigabit network, the relevant pins can be reused for other functions such as GPIO, etc. (Please contact sales personnel for firmware customization).

MAC1 network circuit is as follows:



MAC2 network circuit is as follows:





Note:

Since the PHY configuration address of SOM-ET-AM62 is 0x04, the PHY address on the baseboard cannot be configured as 0x04 to avoid conflicts. It is also not recommended to use addresses 0x00 and 0x01, as these addresses have special purposes in the driver.

4.5 USB

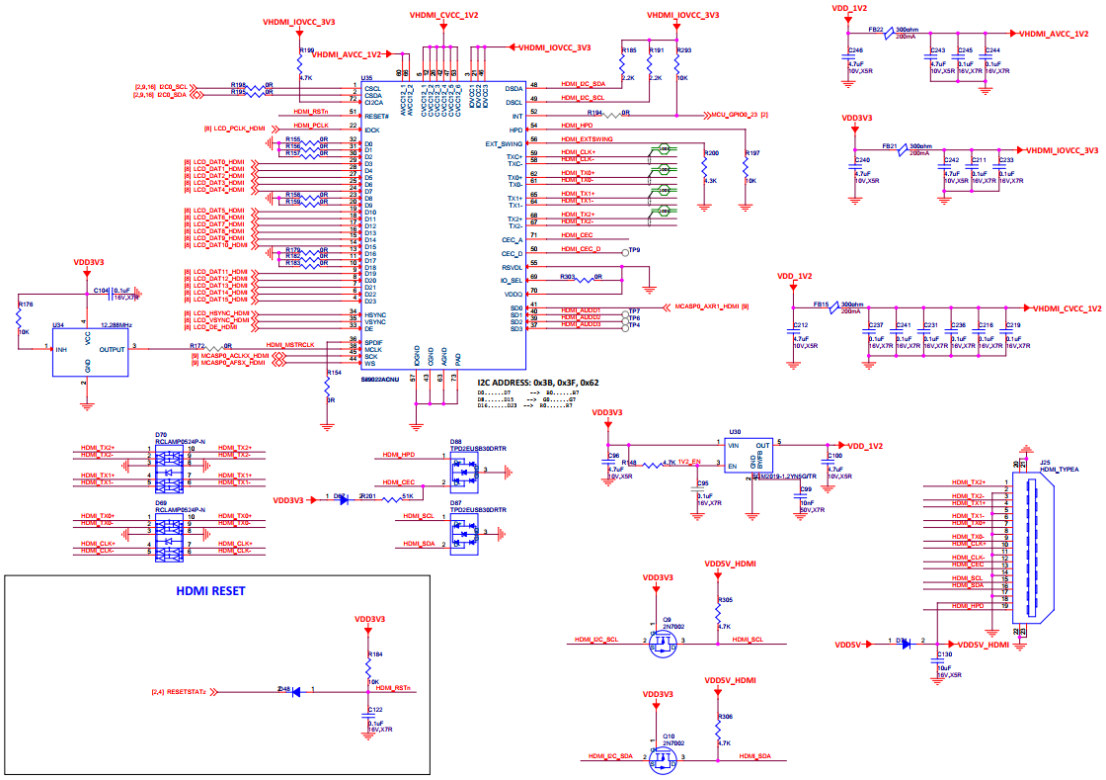
1、 There are no special design requirements for the USB circuit section. Please decide whether to add an external HUB circuit as needed.

2、 Since the TI AM623x/5x series SOC does not support OTG functionality, the SOM-ET-AM62 also cannot support OTG functionality and is designed to use USB as either a Host or Device.

4.6 LCD

The SOM-ET-AM62 provides a parallel LCD output interface, which can offer either 16-bit mode or 24-bit mode output. Since the high 8 bits of display data in 24-bit mode are multiplexed with the GPMC interface, to ensure the integrity of the GPMC functionality, the EVK-ET-AM62 only uses the LCD interface as a 16-bit output. Baseboard design engineers can design the LCD interface as either 16-bit or 24-bit mode according to their needs.

Meanwhile, the EVK-ET-AM62 baseboard uses a Lattice/SII9022 chip to convert the LCD to HDMI output. The specific circuit is as follows:



4.7 LVDS

The TI AM623x/5x provides a multifunctional differential display interface OLDI interface, and the SOM-ET-AM62 uses this interface as LVDS, supporting single-channel or dual-channel LVDS display functionality. The maximum supported resolution is

1920x1080p@60fps.

Meanwhile, backlight control and I2C touch interfaces are reserved:

J4.31 ----> Backlight Enable;

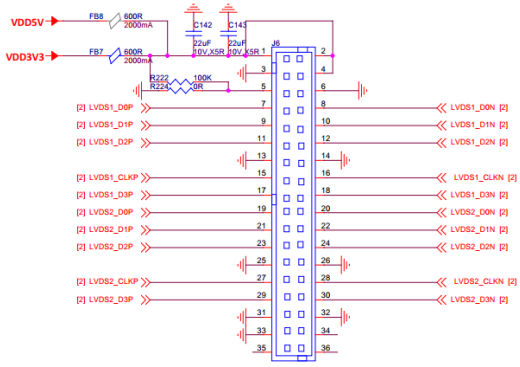
J4.21 ----> Backlight PWM;

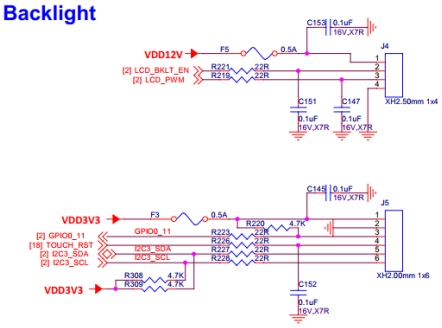
J1.47 ----> Touch I2C Interface SDA;

J1.49 ----> Touch I2C Interface SCL;

J4.26 ----> Touch Interrupt Input;

The LVDS circuit diagram is as follows:

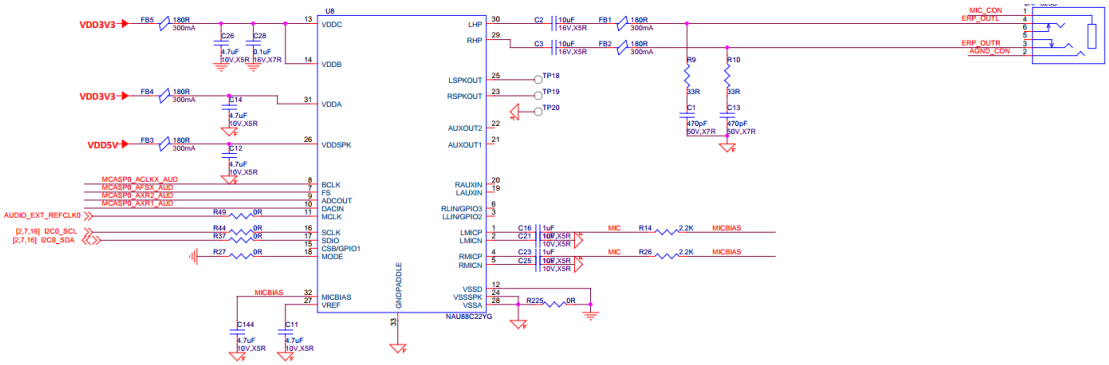




4.8 Audio

The SOM-ET-AM62 provides one MCASP interface for audio expansion. Users can design an audio decoder to implement audio input and output functions according to actual functional requirements.

The audio circuit of the EVK-ET-AM62 is as follows:

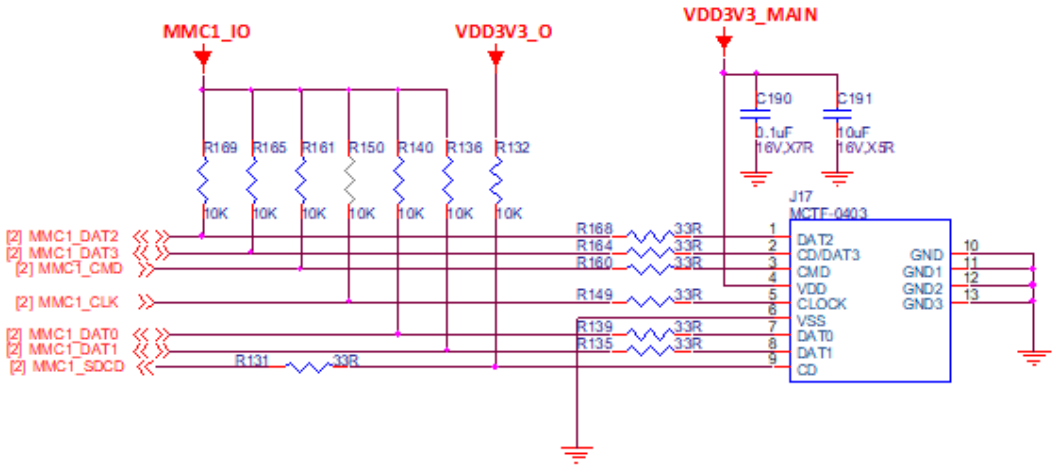


4.9 SDIO

The SOM-ET-AM62 provides two SDIO interfaces, one 4-bit and one 8-bit, which can be used to expand SDIO-related peripherals.

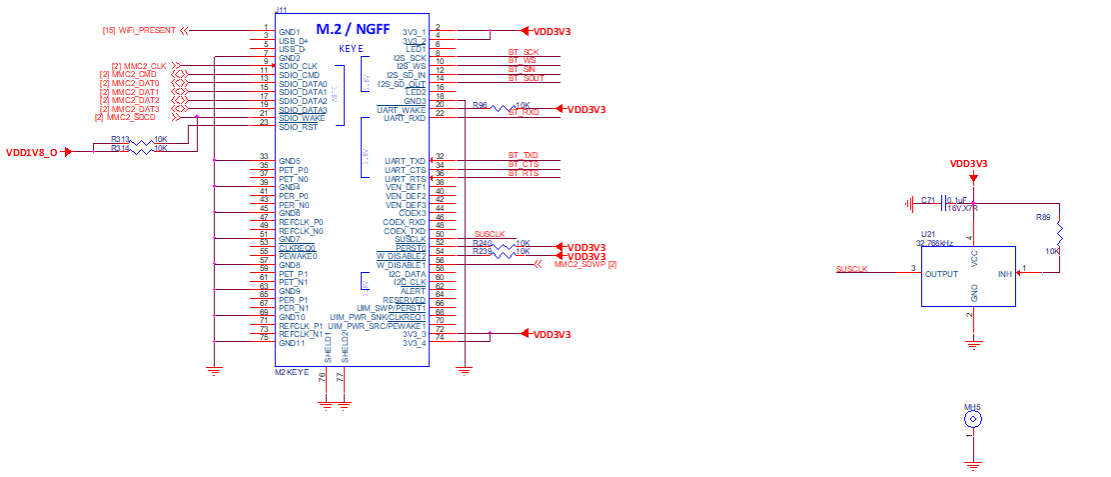
The 4-bit interface is MMC1, and the IO port level is output by the core board and is software controllable. If designed for storage card functionality and requires booting from the storage card, the storage card must be powered by the same power supply as the core board. If the peripheral does not use 3.3V power supply, ensure that the peripheral power supply and the core board's 3.3V power supply start simultaneously to ensure boot functionality.

The design for the card section in the EVK-ET-AM62 is as follows:



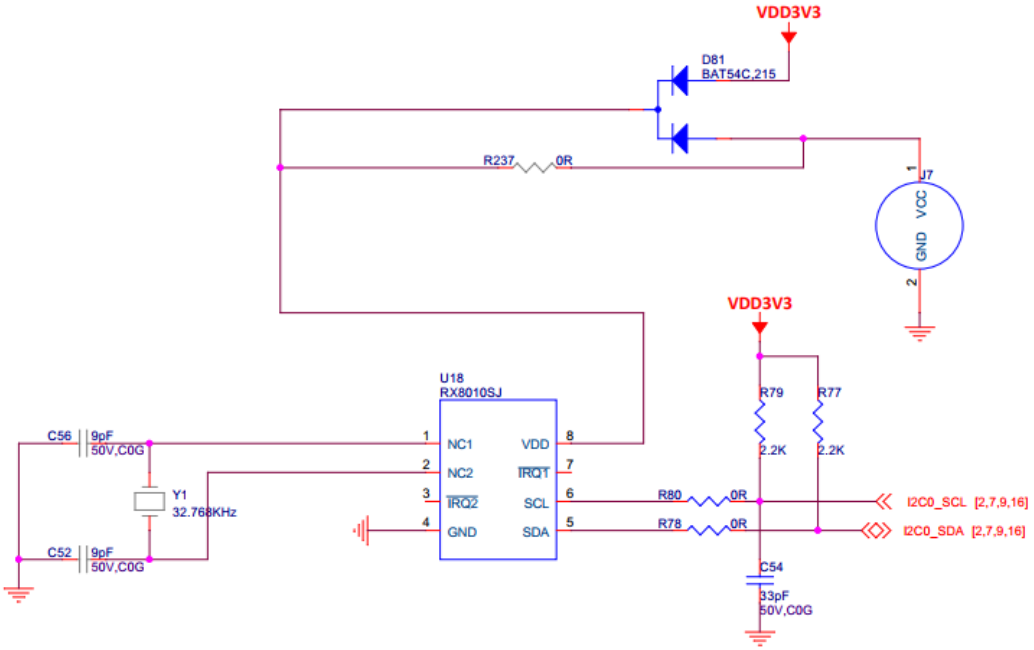
The 8-bit interface is MMC2, with IO power level input from the baseboard. Pin J4.9 is the power pin for the MMC2 interface and must be connected to the appropriate power supply. It is recommended to obtain 1.8V (J4.11) or 3.3V (J4.5) from the power output of the core board.

The EVK-ET-AM62 uses this interface as a communication interface for an external M2 E Key module, the circuit is as follows:



4.10 RTC

Since the TI AM623x/5x does not have a built-in RTC power supply circuit, the CPU's internal RTC module cannot provide power-off preservation functionality. If the customer's design requires the RTC to have power-off operation functionality, an external RTC module is needed. Common external RTC modules use I2C for communication. The EVK-ET-AM62 has designed a simple external RTC module, and its circuit is as follows:



4.11 MIPI CSI

The SOM-ET-AM62 connects all 4Lane MIPI CSI differential lines of the AM623x/5x to the baseboard, using a 15Pin 1.00mm FPC connector. The default supported sensor is the OV5640.

The MIPI CSI circuit is as follows:

